R4000/4400 JTAG Specification Addendum

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1.0 Background information

This document discusses the following topics:

a) JTAG specification related issues not discussed in the R4000/R4400 User's Manual

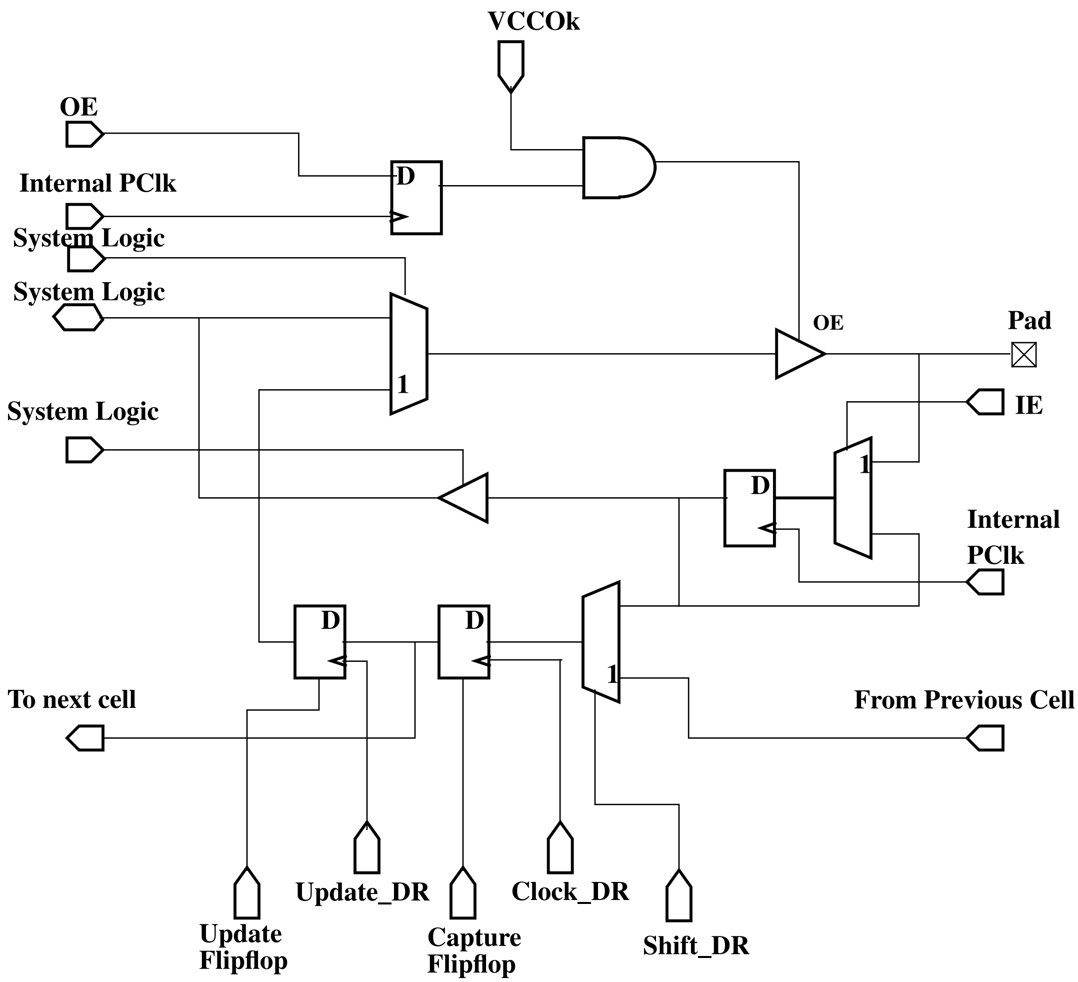
b) How the implementation in the R4000/R4400 deviates from the IEEE Std 1149.1-1990 spec

It is assumed that the reader of this note is familiar with the IEEE JTAG specification as well as with the R4000/R4400 JTAG interface specification from the R4000/R4400 User's Manual.

2.0 Boundary Scan cell

The R4000/R4400 Boundary scan uses the following basic cell type (see Figure 1):

FIGURE 1. R4000/R4400 Boundary Scan cell



2.1 General Operation

The Capture flip-flop gets its input data from the System Input pad after it has been latched into an internal processor clock based flip-flop. The control signal IE enables loading this input flip-flop from the System input pad. The Capture flip-flop is loaded during the Capture_DR and Shift_DR states when the JTAG instruction EXTEST is selected (as per the JTAG definition).

The Update flip-flop gets loaded from the Capture flip-flop during the Update_DR state when the JTAG instruction EXTEST is selected (as per the JTAG definition).

During the EXTEST instruction, the data from the Update flip-flop is selected as the output data; otherwise the output data comes from the internal logic of the chip. The output data is sent out onto the System pad through a tristate buffer. The output enable for the tristate buffer comes from an internal processor clock based flip-flop. The signal OE, which is the input to this flip-flop controls the output enabling of data.

The two control signals that differentiate the above cell for the various R4400 pad types are the IE and OE signals. In the following sections we will describe the operation of the Boundary Scan cell for the various pads.

2.2 Input pads

For the input pads, the control signal IE is an “or” function of the ColdReset input signal and some internal logic generated control (for regular chip operation). Therefore for the JTAG Capture flip-flop to be able to capture the pad data reliably, the Boundary Scan EXTEST instruction must be performed only while the chip is in ColdReset mode (i.e. ColdReset* and Reset* pins are both asserted). Note that a Boundary Scan register bit is associated with each of the VCCOk, ColdReset* and Reset* pads. However since VCCOk serves as the asynchronous reset for the TAP controller, and because of the requirement that input data can only be captured reliably during Coldreset, during the EXTEST instruction, these input pins must always be asserted (i.e. VCCOk=”1”, ColdReset*=”0”, Reset*=”0”).

The IE control for the VCCOk, ColdReset*, Reset*, IOIn and ModeIn pads is a logic “1”. For the rest of the inputs it is as described above.

The OE control for all input pads is a logic “0”.

2.3 Output pads

For most of the output pads, the IE signal is the same as the input pads; i.e an “or” function of the ColdReset and internal logic. However for the SCAddr, SCAPar, SCWR*, SCOE*, SCDCS*, SCTCS*, Fault* and Status pads, the IE signal is purely internal logic controlled. That means the data “captured” in the Capture flip-flop for output pads is generally unreliable, even during ColdReset. This however should not matter for EXTEST purposes. The Capture flip-flops in the TClock, RClock and ModeClock pads always capture a logic “0”, as these pads do not have an input data flip-flop.

The OE signal for output pads is an “or” function of EXTEST (for Boundary Scan operation) and some internal logic generated control (for regular chip operation). So during EXTEST, the Update flip-flop data is always enabled onto the system pad. The TClock, RClock, ModeClock and IOOut pads do not have the latched OE control. In the case of TClock, RClock and IOOut, the output tristate buffer is output enabled by VCCOk; the ModeClock is always output enabled.

2.4 Bidirectional pads

The IE signal for all Bidirectional pads (SysAD, SysADC, SysCmd, SysCmdP, SCData, SCDChk, SCTag, SCTChk) is an “or” function of EXTEST (for Boundary Scan operation) and some internal logic generated control (for regular chip operation). Therefore the pad data is always captured in the Capture flip-flop of bidirectional pads during the Capture_DR state.

The OE signal is selected by the EXTEST function.When EXTEST is a “1” the OE signal comes from the Boundary Scan control cells that control the directionality of the pins (i.e. for SCData and SCDChk OE = SCData_OE, for SCTag and SCTChk OE = SCTag_OE, for SysAD, SysADC, SysCmd and SysCmdP OE = SysAD_OE). When EXTEST is “0” the OE signal comes from internal system logic for the regular operation of the chip.

2.4.1 Control Cells

Each of the 3 control cells for the bidirectional pads, consist of the capture flip-flop and the update flip-flop only. The capture flip-flop captures a “0” during the Capture_DR state, and shifts in the appropriate values during the Shift_DR state. The Update flip-flop gets loaded with the data in the Capture flip-flop in the Update_DR state. The output of the Update flip-flop is the “OE” value (i.e. SCData_OE, SCTag_OE and SysAD_OE).

3.0 Deviations from the IEEE Std 1149.1-1990 spec.

The R4000/R4400 deviates from the following rules of the IEEE Std 1149.1-1990 specification. Some of the rules are totally not followed, and others are violeted partially.

3.3.1(b), 3.4.1(b), 3.5.1(b), 5.2.1(c), 5.2.1(d), 5.3.1(b), 6.1.2(b), 6.2.1(d), 6.2.1(e), 7.2.1(b), 7.6.1(a), 7.7.1(d), 7.7.1(e), 8.3.1(e), 10.1.1(a), 10.1.1(e), 10.3.1(a), 10.4.1(a), 10.5.1(a), 10.6.1(a).

The following is a short summary description of all the above violations.

- The JTMS and JTDI inputs do not have a default pull-up resistor. They need to always be connected externally.
- The JTDO output changes on the falling edge of JTCK in the cycle *following* the Shift_DR or Shift_IR states (i.e. one cycle later than the spec).
- The JTDO output is active in the Capture_IR, Pause_IR, Exit1_IR, Exit2_IR, Capture_DR, Pause_DR, Exit1_DR and Exit2_DR states in addition to the Shift_IR and Shift_DR states.
- The parallel output latches in the Boundary Scan register and the Instruction register are updated on the *rising* edge of JTCK in the Update_DR and Update_IR states respectively.
- There is no support for the Sample/Preload instruction.
- The VCCOk pin is used as the asynchronous reset for the TAP controller; the ColdReset* and Reset* pins need to be asserted for the Boundary Scan register to be used.
- Some pads do not have a Boundary Scan cell and some pads share a single Boundary Scan cell as described in the User’s manual.

- The data coming into the chip from the pad is first latched into an internal processor clock based register before it gets to the Capture flip-flop. The Output Enable control for data going off-chip is first latched into an internal processor clock based register before it actually controls the tristate buffer.